**HO CHI MINH UNIVERSITY OF TECHNOLOGY**

**OFFICE FOR INTERNATIONAL STUDY PROGRAMS - OISP**

**Logic Design with HDL**

EXPERIMENT

**Introduction & Structural Model**

**Group information:**

| Class : Logic Design with HDL (Lab)  Group : 2 | Lecturer’s comment |
| --- | --- |
| Full name:   1. Nguyễn Văn Bình : 2153223 2. Lê Minh Quý : 2153758 3. Trần Hải Đăng : 2153297 4. Phạm Đức Trung : 2153928 |  |

**1 Introduction**

**1.1 Aims**

• Get familiar with Vivado software and the FPGA development flow.

• Get familiar with FPGA Arty-Z7 board.

• Practice in designing simple digital logic circuits with Verilog.

• Understand the hierarchical design principle.

• Practice in writing test benches for a designed module.

**1.2 Preparation**

• Read the laboratory materials before class.

• Revise chapter 0-3 about Verilog basic.

• Each group prepares at least one laptop with Vivado software installed.

**1.3 Documents and lab materials**

• M. Morris Mano, Michael D. Ciletti, Digital System with an Introduction to the Verilog HDL, VHDL,

and SystemVerilog, Pearson Education, Inc, 2017

• Lecture slides

• Arty-Z7-20-Master.xdc: Arty-Z7 constraint file.

• Guide for Installing Vivado.pdf : Guide for installing Vivado and getting started with Vivado and

Arty-Z7.

• dec1to2.v, mux2to1.v : 2-to-1 multiplexer module and its sub-module.

• mux2to2 tb.v: test bench to simulate the module mux2to1.

**1.4 Procedure**

For each exercise (also for further labs):

• Read the requirements, then determine the input/output signals of your circuits.

• Make a design idea of the circuit then use Verilog to model the circuit.

• Analysis & Synthesis the circuit with Vivado software.

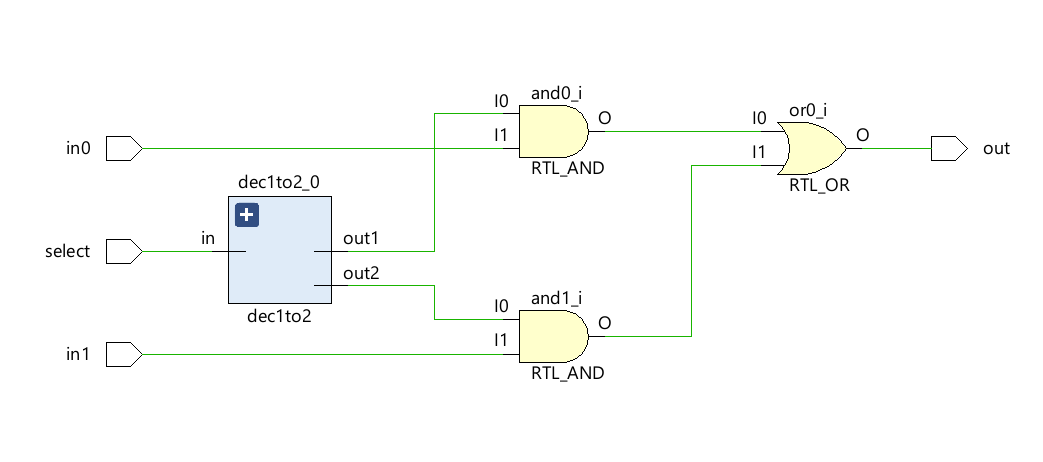
• Write test bench to simulate the circuit on Vivado Simulator.

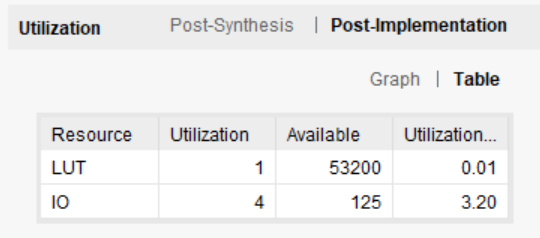
• Generate the bitstream and program the Arty-Z7 to evaluate the circuit.

**2 Exercises**

**2.1 Exercises 1**

- Name of source files : mux2to1.v, dec1to2.v

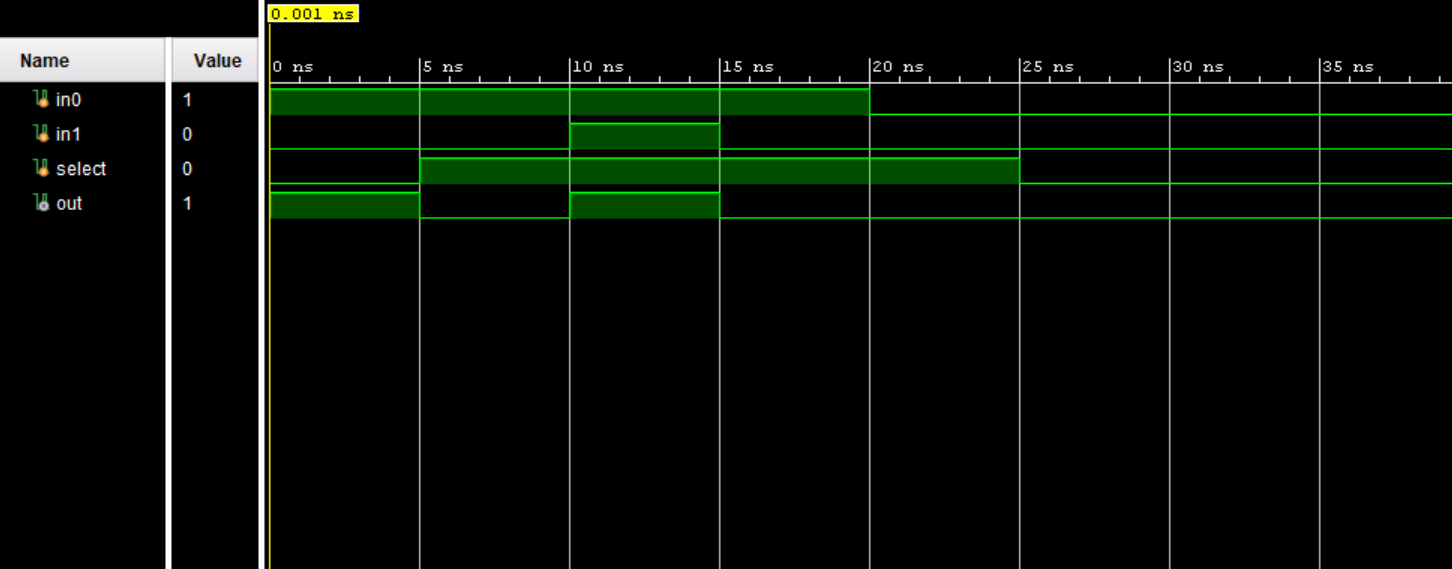
- RTL Schematic

-Resource Utilization 

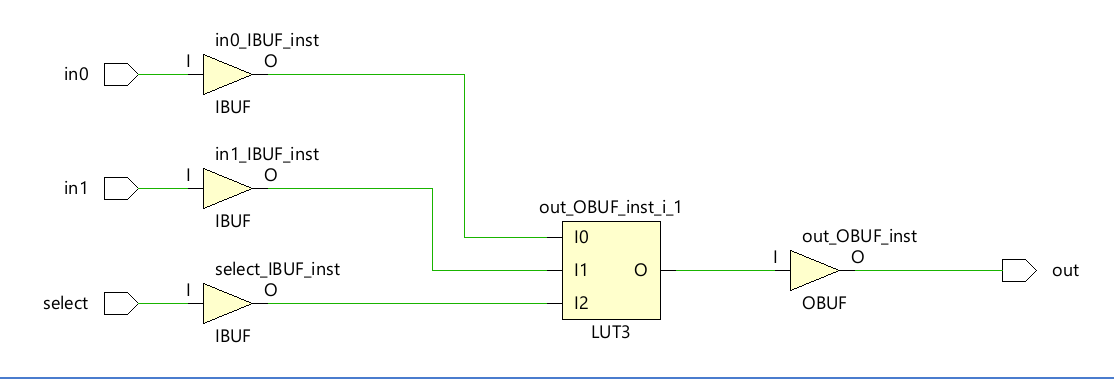
**2.2 Exercises 2**

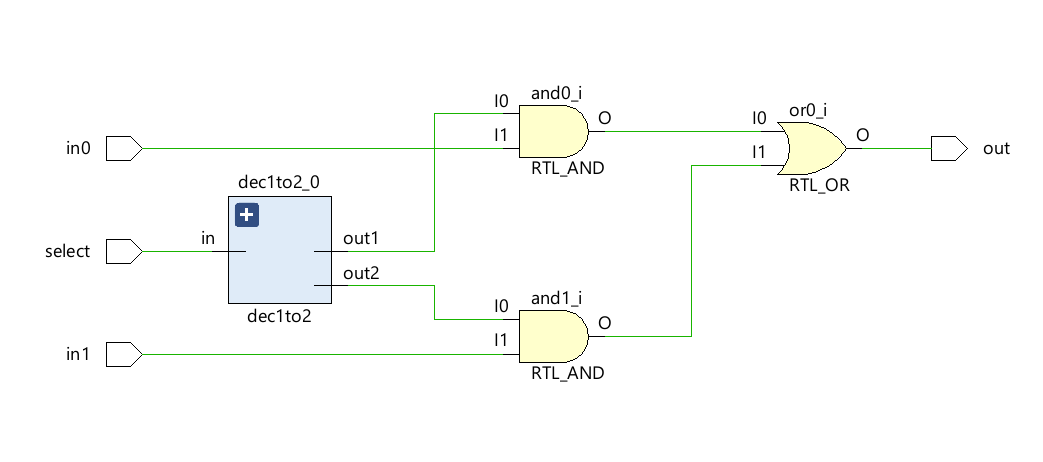
- Source files : mux2to1\_tb.v

- Waveform



Synthesis’s schematic:





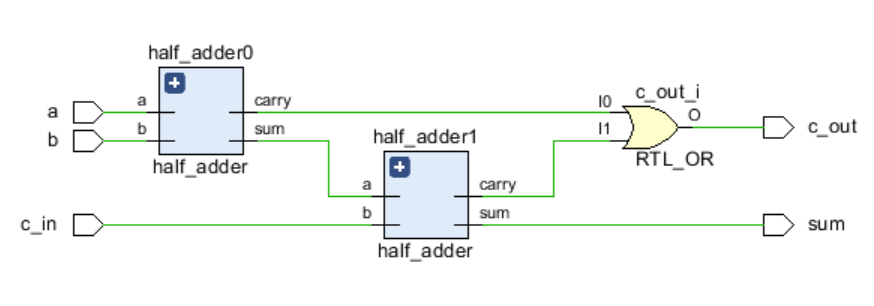
* Compare RTL’s and Synthesis’s schematic: RTL View shows the representation of your design in terms of generic symbols like AND Gates, OR Gates, adders, multipliers etc. Synthesis View shows the representation of your design in terms of logical elements like LUTs, buffers, I/Os, and other technological components.

**2.3 Exercises 3**

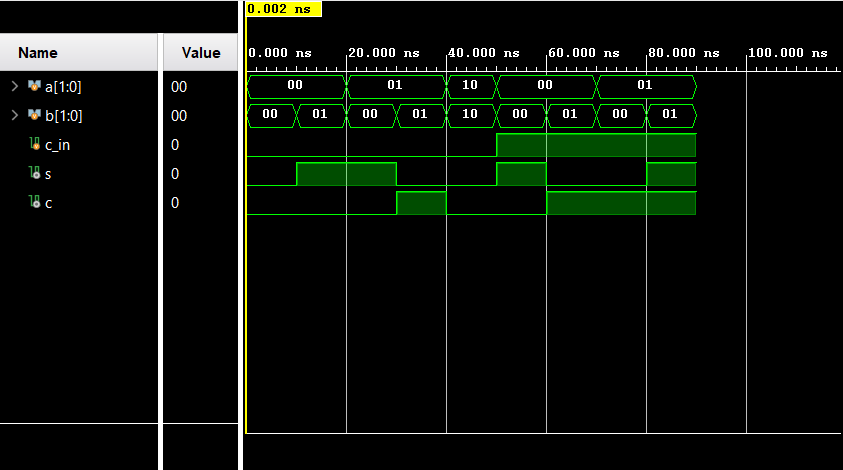
2.3 a,b.

- Name of source files : half\_adder.v, full\_adder.v

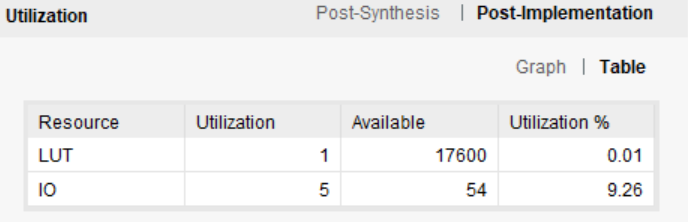
- RTL Schematic



- Waveform



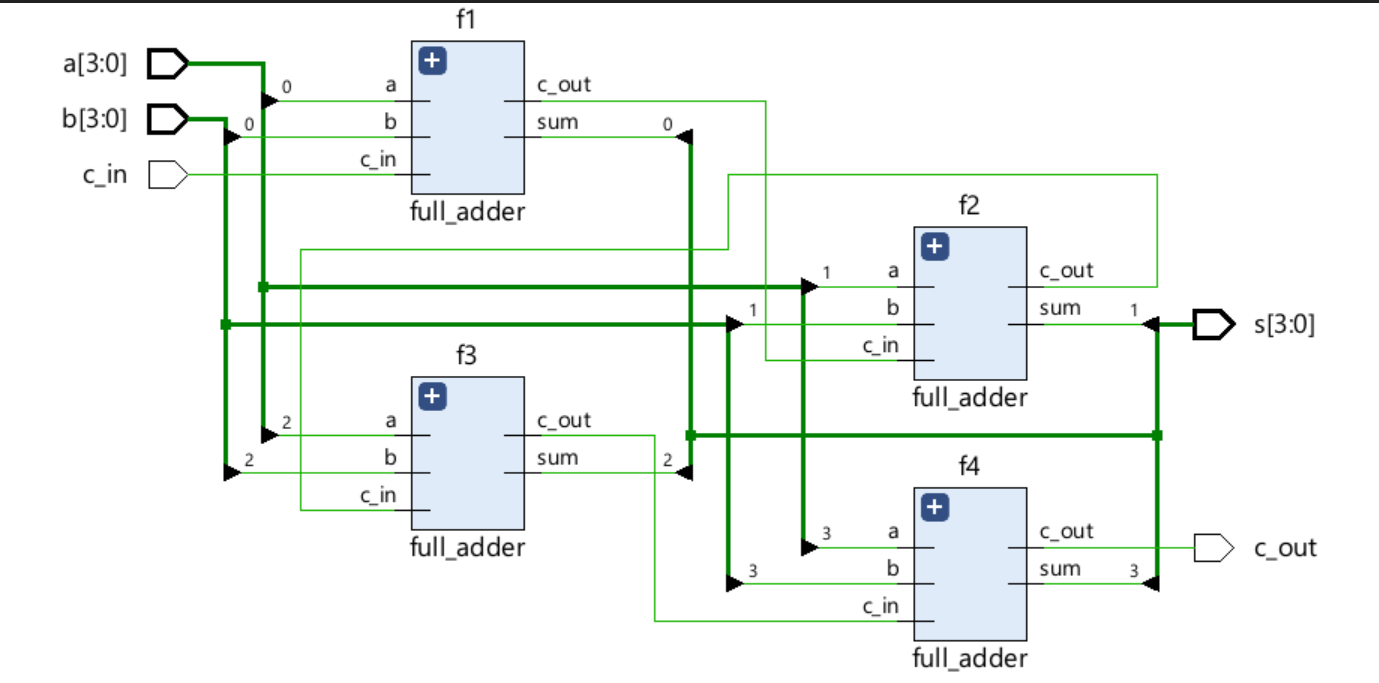
* Resource Utilization



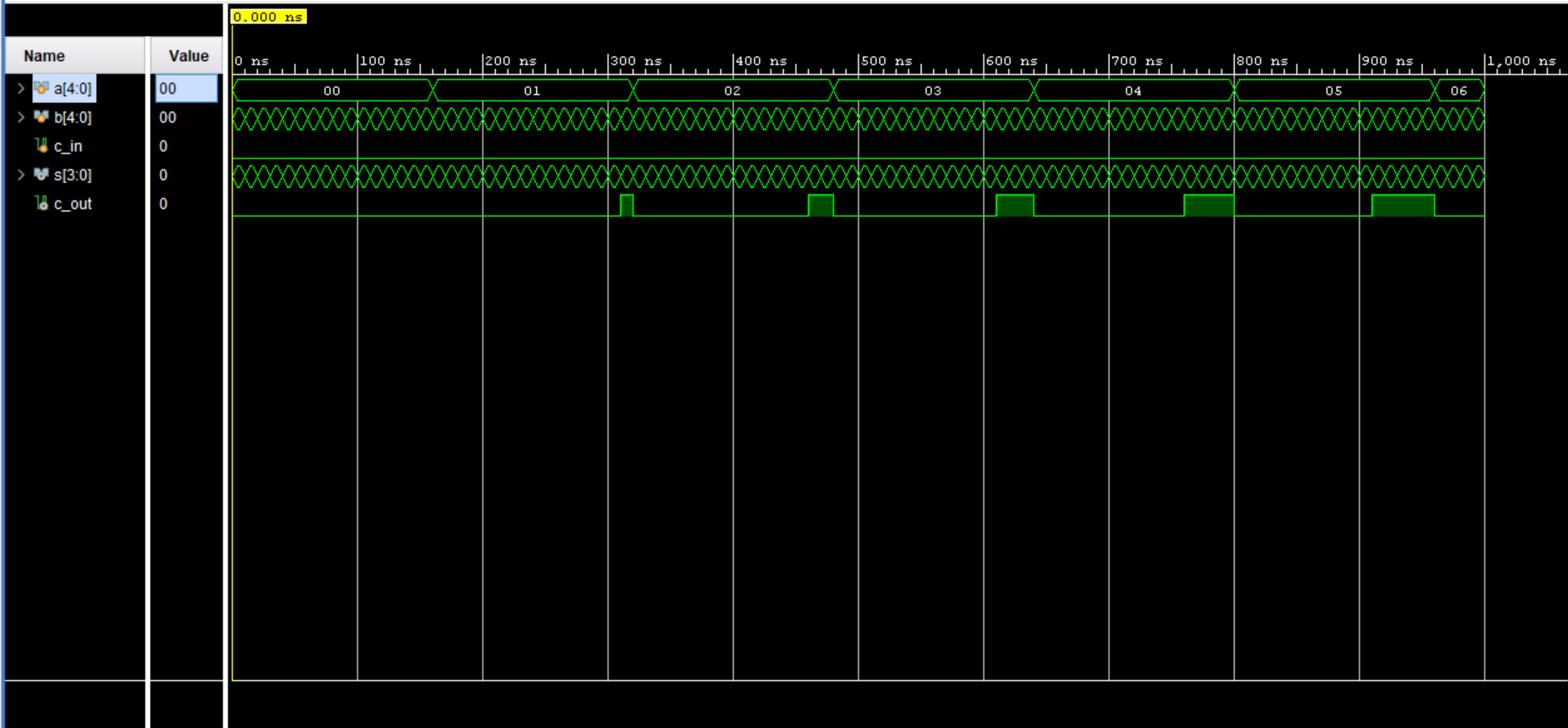
2.3 c

- Name of Source Files : adder4b.v, adder4b\_tb.v

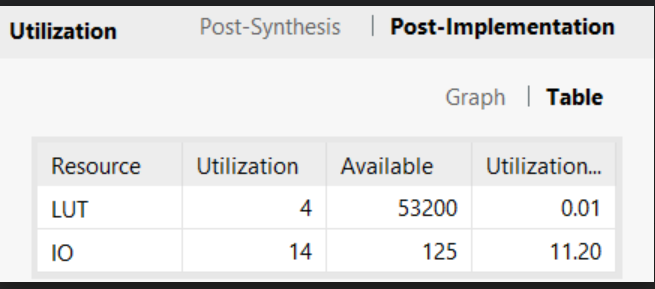
- RTL Schematic



- Waveform



- Resource Utilization



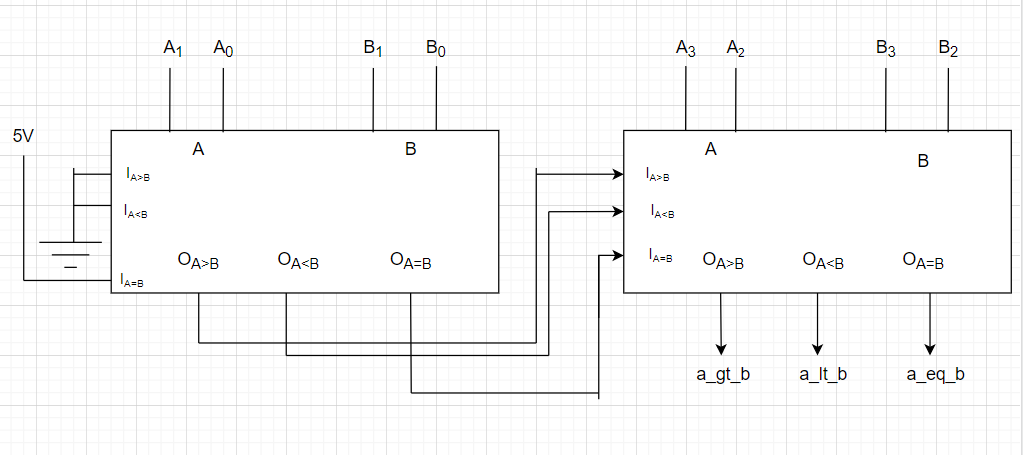
**2.4 Exercises 4**

- Source files : 2bit.v, 4bit.v, test.v

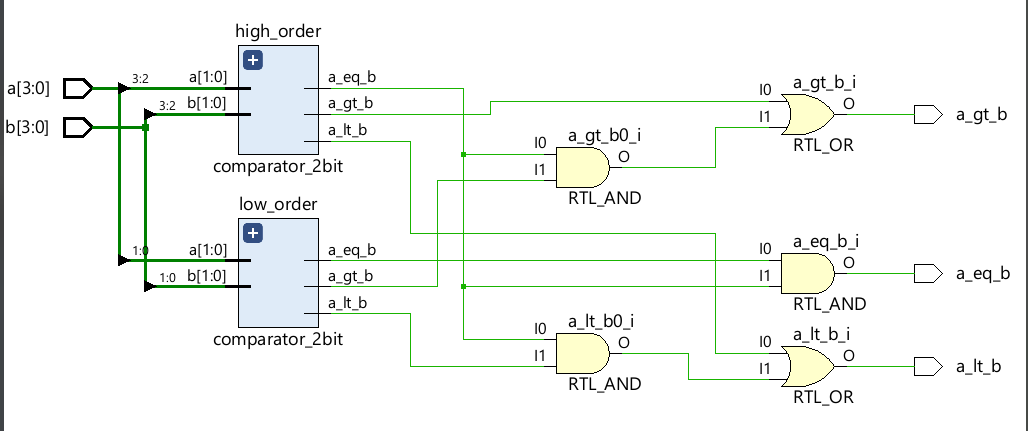
- Analyse the functions of each output of the 2-bit comparator, then determine the functions of 4-bit

comparator outputs:   
The 2-bit comparator reads 2 inputs and compares these values. After that, it returns the result whether A>B or A<B or A=B

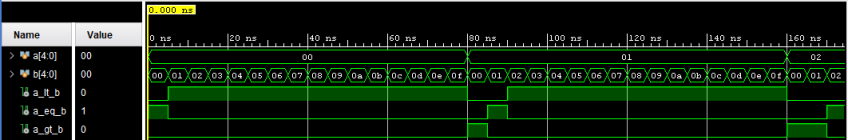
- A block diagram describes the idea:



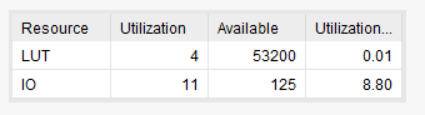
- RTL Schematic



- Waveform



- Resource Utilization



**End.**